AMENDMENTS TO THE CLAIMS

34. (NEW) A semiconductor storage device comprising:

a memory cell array employing a memory element as a memory cell wherein the memory element is constructed of a gate electrode formed via a gate insulation film on a semiconductor layer, a channel region arranged under the gate electrode, diffusion regions that are arranged on both sides of the channel region and have a conductive type opposite to that of the channel region and memory function bodies that are formed on both sides of the gate electrode and have a function to retain electric charges; and

a lockout circuit that inhibits a command to a memory circuit including the memory cell array when a power voltage supplied from outside is lower than a prescribed voltage.

35. (NEW) The semiconductor storage device as claimed in claim 34, wherein

the power voltage supplied from the outside is comprised of at least a first power voltage supplied to the memory circuit including the memory cell array and a second power voltage supplied to an output circuit (35), and

the lockout circuit comprises:

a voltage detector that outputs a first lockout signal for inhibiting the command to the memory circuit including the memory cell array when the first power voltage is not higher than a first prescribed voltage; and

a power voltage confirmation circuit that outputs a second lockout signal for inhibiting the command to the memory circuit including the memory cell array when the second power voltage is lower than a second prescribed voltage.

36. (NEW) The semiconductor storage device as claimed in claim 35, wherein

the power voltage confirmation circuit outputs a lockout signal for inhibiting the command to the memory circuit including the memory cell array when the first power voltage is lower than the first prescribed voltage.

37. (NEW) The semiconductor storage device as claimed in claim 35, comprising:

a comparator that compares the second power voltage with the second prescribed voltage and outputs a signal representing the fact that the second power voltage is higher than the second prescribed voltage to the power voltage confirmation circuit when the second power voltage is higher than the second prescribed voltage.

38. (NEW) The semiconductor storage device as claimed in claim 35, wherein

the voltage detector outputs a signal representing the fact that the first power voltage is lower than the first prescribed voltage to the power voltage confirmation circuit when the first power voltage is lower than the first prescribed voltage.

39. (NEW) The semiconductor storage device as claimed in claim 35, wherein

the power voltage confirmation circuit confirms the second power voltage upon receiving a signal representing the fact that the command is given to the memory circuit including the memory cell array.

40. (NEW) The semiconductor storage device as claimed in claim 39, wherein

the power voltage confirmation circuit outputs a signal representing a result of the confirmation of the second power voltage according to the signal representing the fact that the command is given to the memory circuit including the memory cell array.

41. (NEW) The semiconductor storage device as claimed in claim 35, wherein

the second prescribed voltage is within a range of 0.3 V to 1.2 V.

42. (NEW) The semiconductor storage device as claimed in claim 35, wherein

the command to the memory circuit including the memory cell array is inhibited when at least one of the first lockout signal from the voltage detector and the second lockout signal from the power voltage confirmation circuit is outputted.

43. (NEW) The semiconductor storage device as claimed in claim 35, wherein

a supply state of the power voltage of the voltage detector is controlled by the first power voltage.

44. (NEW) The semiconductor storage device as claimed in claim 37, wherein

a voltage generator circuit for generating the second prescribed voltage is provided, and

the supply state of the power voltages of the comparator and the voltage generator circuit are controlled by the second power voltage.

45. (NEW) The semiconductor storage device as claimed in claim 34, comprising:

power supply switches that are turned on when the memory circuit including the memory cell array is in an active state to supply the power voltage to at least the memory circuit including the memory cell array and turned off when the memory circuit is in a standby state to stop the supply of the power voltage to at least the memory circuit including the memory cell array.

46. (NEW) The semiconductor storage device as claimed in claim 45, wherein

the power voltage supplied from the outside is comprised of at least the first power voltage supplied to the memory circuit including the memory cell array and the second power voltage supplied to the output circuit, and

the lockout circuit comprises:

a voltage detector that outputs a first lockout signal for inhibiting the command to the memory circuit including the memory cell array when the first power voltage is not higher than the first prescribed voltage; and

a power voltage confirmation circuit that outputs a second lockout signal for inhibiting the command to the memory circuit including the memory cell array when the second power voltage is lower than the second prescribed voltage.

47. (NEW) A semiconductor storage device comprising:

power supply switches that stop supplying at least one of a plurality of power voltages supplied from outside when a memory circuit including a memory cell array is in a standby state; and

a lockout circuit that inhibits a command to the memory circuit when any one of the plurality of power voltages is lower than a prescribed voltage.

48. (NEW) A semiconductor storage device control method for inhibiting a command to a memory circuit including a memory cell array, comprising the steps of:

stopping supply of at least one of a plurality of power voltages supplied from outside when the memory circuit is in a standby state; and

inhibiting the command to the memory circuit when any one of the plurality of power voltages is lower than a prescribed voltage.

49. (NEW) A semiconductor storage device control method for inhibiting a command to a memory circuit including a memory cell array, comprising the steps of:

investigating whether or not the memory circuit is in a standby state;

stopping supply of the power voltage to the memory circuit and inhibiting the command to the memory circuit when the memory circuit is in the standby state;

confirming at least one of the plurality of power voltages by a power voltage confirmation circuit; and

outputting a lockout signal for inhibiting the command from the power voltage confirmation circuit to the memory circuit when any one of the plurality of power voltages is lower than a prescribed voltage.

50. (NEW) The semiconductor storage device control method as claimed in claim 49, wherein

the command is a rewrite command.

51. (NEW) The semiconductor storage device control method as claimed in claim 49, wherein

at least one of the plurality of power voltages is compared with the prescribed voltage by a comparator .

52. (NEW) The semiconductor storage device control method as claimed in claim 51, wherein

supply states of power voltages of the comparator and a voltage generator circuit for generating the prescribed voltage are controlled by a first power voltage supplied to the memory circuit including the memory cell array among the plurality of power voltages.

53. (NEW) The semiconductor storage device control method as claimed in claim 49, wherein

a voltage detector detects whether or not a first power voltage supplied to the memory circuit including the memory cell array among the plurality of power voltages is outside a predetermined range, and

a lockout signal for inhibiting the command to the memory circuit is outputted from the voltage detector when the first power voltage is outside the predetermined range.

54. (NEW) The semiconductor storage device control method as claimed in claim 53, wherein

the command to the memory circuit including the memory cell array is inhibited when at least one of the lockout signal from the voltage detector and the lockout signal from the power voltage confirmation circuit is outputted.

55. (NEW) The semiconductor storage device control method as claimed in claim 53, wherein

the supply state of a power voltage of the voltage detector is controlled by the first power voltage.

56. (NEW) The semiconductor storage device control method as claimed in claim 49, wherein

the lockout signal for inhibiting the command to the memory circuit is outputted from the power voltage confirmation circuit when the power voltage supplied to the output circuit among the plurality of power voltages is lower than the prescribed voltage.

57. (NEW) The semiconductor storage device control method as claimed in claim 49, wherein

the plurality of power voltages are confirmed by the power voltage confirmation circuit.

58. (NEW) The semiconductor storage device control method as claimed in claim 57, wherein

the command to the memory circuit including the memory cell array is inhibited on the basis of at least one of the plurality of power voltages.

59. (NEW) The semiconductor storage device control method as claimed in claim 57, wherein

the lockout signal for inhibiting the command to the memory circuit is outputted from the power voltage confirmation circuit when the power voltage supplied to the memory circuit including the memory cell array among the plurality of power voltages is outside a predetermined range.

60. (NEW) The semiconductor storage device control method as claimed in claim 56, wherein

the prescribed voltage for determining the power voltage supplied to the output circuit among the plurality of power voltages is within a range of 0.3 V to 1.2 V.

61. (NEW) A semiconductor storage device comprising:

a memory cell array employing a memory element as a memory cell wherein the memory element is constructed of a gate electrode formed via a gate insulation film on a semiconductor layer, a channel region arranged under the gate electrode, diffusion regions that are arranged on both sides of the channel region and have a conductive type opposite to that of the channel region and memory function bodies that are formed on both sides of the gate electrode and have a function to retain electric charges; and

power supply switches that are turned on to supply the power voltage to at least the memory circuit including the memory cell array when the memory circuit is in an active state and that are turned off to stop the supply of the power voltage to at least the memory circuit including the memory cell array when the memory circuit is in a standby state.

62. (NEW) The semiconductor storage device as claimed in claim 61, wherein

the power supply switches are formed on a substrate identical to that of the memory circuitincluding the memory cell array.

63. (NEW) The semiconductor storage device as claimed in claim 34, wherein at least part of the memory function bodies possessed by the memory element overlaps with part of a diffusion region.

64. (NEW) The semiconductor storage device as claimed in claim 47, wherein at least part of the memory function bodies possessed by the memory element overlaps with part of a diffusion region.

65. (NEW) The semiconductor storage device as claimed in claim 61, wherein at least part of the memory function bodies possessed by the memory element overlaps with part of a diffusion region.

66. (NEW) The semiconductor storage device as claimed in claim 34, wherein there is provided an insulation film for isolating from the channel region or the semiconductor layer a film which has a surface roughly parallel to a surface of the gate insulation film of the memory element and has a function to retain electric charges, and a film thickness of the insulation film is thinner than a film thickness of the gate insulation film and is not smaller than 0.8 nm.

67. (NEW) The semiconductor storage device as claimed in claim 47, wherein there is provided an insulation film for isolating from the channel region or the semiconductor layer a

film which has a surface roughly parallel to a surface of the gate insulation film of the memory element and has a function to retain electric charges, and a film thickness of the insulation film is thinner than a film thickness of the gate insulation film and is not smaller than 0.8 nm.

68. (NEW) The semiconductor storage device as claimed in claim 61, wherein there is provided an insulation film for isolating from the channel region or the semiconductor layer a film which has a surface roughly parallel to a surface of the gate insulation film of the memory element and has a function to retain electric charges, and a film thickness of the insulation film is thinner than a film thickness of the gate insulation film and is not smaller than 0.8 nm.

69. (NEW) The semiconductor storage device as claimed in claim 34, wherein the memory function bodies possessed by the memory element comprise a film that has a surface roughly parallel to a surface of the gate insulation film and has a function to retain electric charges.

70. (NEW) The semiconductor storage device as claimed in claim 47, wherein the memory function bodies possessed by the memory element comprise a film that has a surface roughly parallel to a surface of the gate insulation film and has a function to retain electric charges.

71. (NEW) The semiconductor storage device as claimed in claim 61, wherein the memory function bodies possessed by the memory element comprise a film that has a surface

roughly parallel to a surface of the gate insulation film and has a function to retain electric charges.

72. (NEW) Portable electronic equipment employing the semiconductor storage device claimed in claim 34.

73. (NEW) Portable electronic equipment employing the semiconductor storage device claimed in claim 47.

74. (NEW) Portable electronic equipment employing the semiconductor storage device claimed in claim 61.

75. (NEW) Portable electronic equipment control method employing the semiconductor storage device control method claimed in claim 48.

76. (NEW) Portable electronic equipment control method employing the semiconductor storage device control method claimed in claim 49.